L. A. VERHOEF, P-P. MICHIELS, S. ROORDA and W. C SINKE

FOM-Institute for Atomic and Molecular Physics, Kruislaan 407, 1098 SJ Amsterdam (The Netherlands)

R. J. C. VAN ZOLINGEN

R&S Renewable Energy Systems B.V., P.O. Box 45, 5600 AA Eundhoven (The Netherlands)

(Received February 12, 1990)

Abstract

Polycrystalline silicon wafers were subjected to extra thermal treatments (0-120 min, 500-800 °C) during the processing of solar cells. It was found that the bulk effective minority carrier diffusion length was enhanced significantly upon annealing, provided the front and back sides of the wafers were doped with phosphorus and aluminium respectively, prior to the anneal. The optimum anneal temperature was 700 °C, yielding an increase of over 10% in diffusion length and a solar cell efficiency improvement of 0.5% absolute, compared with standard cells. Light-beaminduced current measurements have shown that the thermal treatment is most effective in regions with an initially small minority carrier diffusion length. In a separate model experiment with intentionally contaminated wafers, the concentration of metallic impurities such as gold, nickel and copper in the aluminium-doped layer was found to be 1000 times larger than the solid solubility of these metals in silicon at 700 °C. From these observations, it is concluded that gettering of impurities occurs during the annealing and that the aluminium-doped layer (produced by low cost screenprinting process) provides an effective sink for *impurities*.

1. Introduction

Large-grain polycrystalline silicon (poly-Si) is widely used for the production of silicon solar cells. The major advantage of poly-Si is its low cost relative to monocrystalline silicon (mono-Si). The disadvantages are the significantly smaller minority carrier diffusion length and lifetime compared with mono-Si and the inhomogeneous nature of the material. These two drawbacks, which are due to the presence of grain and subgrain boundaries, large concentrations of dislocations and other physical and chemical defects, result in a smaller poly-Si cell efficiency compared with mono-Si cells.

Various ways to improve poly-Si solar cell efficiency have been pursued in the past. One strategy is to reduce the cell thickness and to employ light trapping concepts [1]. In that way, cell performance becomes less dependent on the minority carrier diffusion length. In a second approach, hydrogen passivation is used to reduce minority carrier recombination at physical defects. It involves the binding of hydrogen atoms to dangling bonds and defected regions which lessens the density of mid-bandgap recombination centres [2, 3]. A third method is gettering of lifetime degrading impurities either at defects and grain boundaries (intrinsic gettering) [4, 5] or at the wafer surface (extrinsic gettering) [6-12]. By extrinsic gettering, recombination centres are actually removed from the active part of the cell.

Gettering techniques may be applied to both poly-Si and mono-Si. The commonly accepted phenomenological picture for extrinsic gettering is the following [7]. First, an impurity atom has to be released from its site in the silicon bulk, then it has to diffuse towards the surface and finally it has to be captured at the surface region. In general, high temperatures are needed to enable both the release and the diffusion of the impurity. Furthermore, a sink for the diffusing impurities has to be present at the surface. Several surface treatments such as phosphorus indiffusion [6, 13], metal film deposition and subsequent annealing [12, 14, 15], Si₃N₄ film deposition followed by a thermal treatment [16, 17], and mechanically damaging the surface [18] have been shown to provide such sinks. It is thought that these treatments may all getter different impurity species and it is speculated that application of several of these gettering treatments is in general more beneficial than utilizing only one [7, 9, 19].

Several models have been developed to describe the gettering mechanism in more detail. In the first model, the surface treatment (e.g.phosphorus indiffusion) is assumed to generate silicon self-interstitials. These interstitials may then react with low mobility, high solubility substitutional metals resulting in interstitial high mobility, low solubility metal atoms, which diffuse very fast towards the surface region where they are captured [20]. Also, the silicon self-interstitials may enhance the effectiveness of the impurity sink by reacting with metals to form surface silicides [21]. In the second model, the solubility of impurities is taken to be larger in highly doped material than it is in the silicon bulk owing to ion pairing [22] and a shift in the Fermi level [23, 24]. A gradient in the solubility (for instance obtained by doping the surface region through diffusion) will be the driving force for gettering. In the third model, it is proposed that the surface treatment results in large concentrations of defects which act as impurity sinks upon annealing [25]. In a recent review, Kang and Schroder [7] concluded that neither of these models fully agree with gettering data and they proposed a new diffusion/segregation model. In this model every gettering treatment has an optimum temperature, below which the gettering efficiency is limited by the diffusion of the impurity. Above that optimum temperature, the ratio of the maximum impurity concentration in the gettering surface region and the bulk impurity solubility limits the efficiency of the gettering treatment.

In low cost solar cell processing of poly-Si material, gettering treatments may be particularly beneficial. In the first place this is because of the larger concentration of metallic impurities present in this material compared with mono-Si [26]. In the second place it is because in low cost processes such as screen-printing, extra impurities might be introduced during standard processing steps. One form of gettering included in most standard silicon solar cell processes occurs as a side effect during the phosphorus indiffusion. Extra gettering steps such as metal film deposition followed by thermal annealing may be added to the production sequence. In one standard processing scheme an aluminium-doped back side is formed by screen-printing and subsequent alloyIng and etching. This aluminium-doped layer may be used as an additional sink for impurities during an extra thermal treatment after the alloying [8-10].

Previous experiments on aluminium-induced gettering have employed evaporated aluminium films and subsequent annealing both below and above the eutectic temperature (577 °C). It was shown that the minority carrier lifetime of cast polycrystalline silicon (Wacker SILSO) was improved after annealing for 2 h at 450 °C [12]. Sundaresan et al. [15] have shown that the minority carrier diffusion length of the same material was enhanced by a 1 h treatment at 700 °C. Enhanced concentrations of impurities have been detected at the Al-Si interface after aluminium film deposition and annealing at 900 °C [27] and also at 540 °C [14] in model experiments on intentionally contaminated mono-Si.

In this paper we report on a series of experiments on phosphorus-induced and aluminiuminduced gettering in which the silicon wafer is doped with aluminium by screen-printing and subsequent firing. The effect of both the annealing temperature and the annealing time have been studied systematically. Furthermore, combined phosphorus-induced and aluminium-induced gettering was studied. In a separate model experiment with intentionally contaminated wafers, the amount of impurities which may be captured in the aluminium-doped layer was investigated.

2. Solar cell fabrication and sample preparation

Polycrystalline silicon cells were fabricated on $10 \times 10 \text{ cm}^2$ Wacker SILSO wafers (doping density 5×10^{15} B cm⁻³, thickness 450 μ m). This material has an average grain size of approximately 5 mm². Most grain boundaries run perpendicular to the wafer surface.

The standard solar cell production scheme is shown in Fig. 1. The wafers are first etched to a thickness of 400 μ m in an alkaline etch to remove the sawing damage. Subsequently, a phosphorus diffusion step (875 °C, 20 min) is carried out resulting in an emitter with a thickness of approximately 0.5 μ m and a surface doping density of about 2 × 10²⁰ cm⁻³. A paste containing aluminium is screen-printed on the back of the wafer and an Al-Si alloy is formed by heating (greater than 700 °C, 4 min) in a belt furnace under the flow of nitrogen gas. The wafers are etched in aqueous HCl to remove most of the Al–Si alloy, leaving behind an aluminium-doped back side (thickness approximately 1.0 μ m, surface doping density of 10¹⁹ cm⁻³). Next, the wafers were etched in aqueous HF to remove SiO₂. An antireflection (AR) coating of Ta₂O₅ (thickness about 70 nm, index of refraction 2.3) is applied. The front metallization finger pattern (coverage 13.6%) and a full back metallization are made by nickel plating and solder dipping.

A number of wafers was subjected to an extra thermal treatment in a belt furnace under flowing nitrogen gas (see Fig. 1). Some wafers received this treatment directly after the phosphorus diffusion. These wafers only contain a phosphorus-doped front surface layer during the anneal and will be labelled as P-groups. Other wafers received the extra anneal just before the AR coating step. These wafers contain both a phosphorus-doped



Fig. 1. Flow diagram of the cell production. The standard processing sequence is denoted by STD. The P-groups received an extra thermal treatment directly after the phosphorus indiffusion, the A-groups received the extra treatment prior to application of the anti-reflection coating.

front region and an aluminium-doped back side during the anneal and will be labelled as A-groups.

Three separate experimental batches were formed (see Table 1): one batch to study the dependence of gettering on temperature, a second batch to evaluate the effect of anneal time, and a third batch to investigate the impact of the extra anneal on the statistical distribution of cell efficiencies. Each batch is randomly selected from a large number (greater than 2000) of wafers and within each batch all groups are statistically equivalent.

The first batch of 125 wafers was divided into five groups of 25 wafers each. Standard cells were produced from one group, the other four (A-) groups received a 1 h anneal at temperatures of 500, 600, 700 or 800 °C, just before application of the AR coating.

From a second batch, 12 groups of 100 wafers were formed. These were all annealed at 700 °C for various times, ranging from 0 to 120 min, either with only phosphorus-doped front or with both aluminium-doped back and phosphorusdoped front. In addition, 25 wafers from a single ingot were distributed over these groups: for each wafer in a certain experimental group, the two adjacent (neighbouring) wafers are allocated to the standard group.

Two large groups of 750 wafers each were formed from a third batch of cells. One of these groups was processed in the standard way; the other group received an additional anneal at 700 °C for 1 h with both aluminium-doped back and phosphorus-doped front side (A-group).

Metallic impurities in Wacker SILSO are present in concentrations smaller than 10^{14} cm⁻³ [28]. The maximum amount which may be gettered at the surface is the product of that concentration and the wafer thickness. This yields 4×10^{12} atoms cm⁻², which is below the detection limit of most techniques. Therefore a model experiment has been conducted to investigate the metallic impurity concentration in the aluminium-

Batch	Number of groups	Number of wafers per group	Temperature	Time	Groups	Values
1 2 3	5 12 2	25 100 750	Variable 700 °C 700 °C	60 min Variable 60 min	A A, P A	0, 500, 600, 700, or 800 °C 0, 7.5, 15, 30, 60, or 120 min

TABLE 1 Experimental matrix

doped layer upon annealing. Monocrystalline CZ silicon wafers (400 μ m thick) were etched in a HNO₃/CH₃COOH/HF mixture in the ratio 7:2:2 to remove the sawing damage and to obtain a flat untextured surface [29]. One set of samples (1×1) cm^2) was doped with aluminium at the back side (by the aforementioned method of alloying and etching); the set of control samples did not receive any surface doping. Metal films (nickel, gold, iron, or copper) 100 nm thick were evaporated on part of the front side of the aluminium-doped and control samples. All samples were annealed at 700 °C under flowing nitrogen gas. Both before and after the anneal (channelled) Rutherford backscattering spectrometry (RBS) [30] measurements were performed on the sample side opposite to the metal-evaporated side using 2 MeV He⁺ ions.

3. Opto-electrical characterization

During processing, the emitter sheet resistance R_{sheet} was determined using a four-point probe on selected wafers from each group both before and after the extra anneal. R_{sheet} depends inversely on emitter thickness W, average active emitter doping concentration $N \ (\text{cm}^{-3})$, and average majority electron mobility μ in the emitter: $R_{\text{sheet}} = 1/(e\mu NW)$, with *e* the electronic charge.

Current-voltage characteristics were measured for all completed cells under a solar simulator with an air mass (AM) 1.5 spectrum and a light power density of 1000 W m⁻² at a cell temperature of 25 °C. From these, the shortcircuit current density I_{sc} , the open-circuit voltage V_{oc} , the fill factor FF, and the efficiency η were determined.

The internal quantum efficiency (QE), defined as the number of electrons in the external current divided by the photon flux which is coupled into the cell, was measured on 10 randomly selected cells from all groups as a function of wavelength in the range 350-1100 nm using interference filters of bandwidth 10 nm. The recombination rate at minority carrier (electron) traps is reduced when the electron quasi-Fermi level shifts owing to generation of electrons [31, 32]. Therefore the quantum efficiency is measured at a white light bias of 1000 W m⁻² (the actual operating conditions of a solar cell) to saturate these traps. From a linear fit of 1/QE vs. $1/\alpha$ for those wavelengths where absorption in the emitter is negligible (800-1000 nm), the effective minority carrier diffusion length $L_{\rm eff}$ is calculated from the ratio of intercept at the $1/\alpha$ axis and the slope [33]. The wavelength-dependent optical absorption coefficient α in silicon was taken from data by Swimm and Dumas [34]. The absolute values of $L_{\rm eff}$ depend on the absorption coefficient data set used, but the relative difference between groups does not.

To investigate the local effective minority carrier diffusion length in standard and annealed cells, light-beam-induced current (LBIC) [35] measurements were performed over large areas on neighbouring cells. A light beam of wavelength 870 nm was focused to a spot of 15 μ m onto the cell and was scanned over the cell surface while measuring the short-circuit current.

4. Results

4.1. Temperature dependence

In Table 2 the results of the I(V) and quantum efficiency measurements are summarized for the A-groups annealed at various temperatures for 1 h. Annealing at 700 °C is optimal for all cell parameters except for the FF. The increases in I_{sc} , V_{oc} , and η with annealing temperature are mainly due to the increase in L_{eff} . I_{sc} and L_{eff} are equal to or smaller than the standard group after an anneal at 800 °C, but for this anneal temperature FF and V_{oc} are still considerably larger than in the standard group. Furthermore, it was found that R_{sheet} increases with annealing temperature to 20% larger than standard at 700 °C but decreases back to its original (standard) value after an anneal at 800 °C.

4.2. Time dependence

Next, anneals were performed for various times at the above-mentioned optimum tempera-

TABLE 2 Results of I(V) measurements under AM1.5, 1000 W m⁻² illumination on the A-groups annealed for 1 h at various temperatures. Averages are over 25 cells for all parameters. Also shown is the effective minority carrier diffusion length $L_{\rm eff}$ derived from internal quantum efficiency measurements

<i>Temperature</i> (°C)	$I_{\rm sc} \ ({\rm mA~cm^{-2}})$	$V_{\rm oc} \ ({ m mV})$	FF (%)	$\stackrel{m{\eta}}{(\%)}$	$L_{\rm eff}$ $(\mu { m m})$
0	25.5	5547	714	10.1	70
500	25.4	555.1	717	101	73
600	25.5	554 5	70.9	100	77
700	25.9	558.0	72.6	10 5	80
800	25.1	556.5	730	102	70



Fig 2. Emitter sheet resistance normalized with respect to the standard group as a function of anneal time at 700 °C.

ture of 700 °C. Prior to application of the AR coating, the sheet resistance of all groups was determined. R_{sheet} increases logarithmically with increasing anneal time to a value which is 25% larger than that of the standard group after annealing for 2 h at 700 °C (Fig. 2).

The results of the I(V) measurements are shown in Fig. 3. By virtue of the relatively large number of cells per group, the absolute errors in $I_{\rm sc}$, $V_{\rm oc}$, FF and η are smaller than 0.04 mA cm⁻², 0.5 mV, 0.2%, and 0.03% respectively. For the groups which have an aluminium-doped back side during the anneal, $I_{\rm sc}$, $V_{\rm oc}$, and η increase with anneal time. FF remains unchanged upon annealing for 7.5 or 15 min but is about 1% (absolute) larger than standard after annealing for 30 min or more. The average cell efficiency obtained in the A-groups after annealing for 1 or 2 h was 10.4% which is 0.5% (absolute) larger than the standard group efficiency. The AR coating was optimized for encapsulation under glass; upon encapsulation, all values for efficiency reported here increased by 0.5% (absolute).

In the P-groups, I_{sc} also increases with increasing anneal time. For these groups, V_{oc} is at least 2.0 mV smaller than the standard group for all anneal times; it is not clear why V_{oc} of the group annealed for 15 min deviates from this behaviour. The fill factor is smaller than standard for all P-groups, but no simple correlation between anneal time and FF is observed: the initial decrease for 7.5 min is followed by a recovery for 15 and 30 min and a further degradation for longer anneal times. This all results in an efficiency which is 0.1% (absolute) smaller than the standard efficiency for the anneal times 7.5, 60, and 120 min, and larger efficiencies for anneal



Fig. 3. (a) Short-circuit current density I_{sc} , (b) open-circuit voltage V_{oc} , (c) fill factor FF, and (d) cell efficiency η of the various groups as a function of anneal time at an anneal temperature of 700 °C. Measurements were performed under illumination with 1000 W m⁻², AM1.5 at a cell temperature of 25 °C.



Fig. 4. Quantum efficiency measurements on groups with (a) both a phosphorus-doped front and aluminium-doped back side and (b) only a phosphorus-doped front side during the anneal at 700 °C. The results have been normalized relative to the standard group A white light bias of 1000 W m⁻² was applied.

times of 15 min (owing to a large V_{oc}) and 30 min (owing to a large FF).

The internal quantum efficiency data, relative to the standard group and averaged over 10 randomly selected wafers per group, are shown in Fig. 4. The error in the average value, shown in one of the curves, is typically less than 1% for all wavelengths. In the A-groups, a clear increase in QE with increasing anneal time (except for 7.5 min) is seen for wavelengths $\lambda > 600$ nm and for $\lambda < 450$ nm (Fig. 4(a)). In the P-groups, this effect is less pronounced or even absent for $\lambda > 600$ nm but more prominent for small wavelengths $\lambda < 450$ nm (Fig. 4(b)). For the P-group annealed for 1 h, a slightly smaller than standard QE is observed in the range between 450 and 800 nm which may be due to small differences in the antireflection coating.

 L_{eff} , determined from QE using the absorption coefficient data from Swimm and Dumas [34],



Fig. 5. Effective minority carrier diffusion length, as determined from the QE of Fig 4, vs anneal time for groups annealed at 700 °C

is shown in Fig. 5. In the A-groups, $L_{\rm eff}$ degrades slightly after 7.5 min, after which it increases with increasing anneal time up to 76.3 μ m after 120 min. In the P-groups, the same initial decrease followed by an increase with anneal time is observed, but this increase is smaller than in the A-groups. $L_{\rm eff}$ of the A-group is smaller than that of the P-group only after 15 min annealing. For all other anneal times, $L_{\rm eff}$ of the A-group is larger than or equal to that of the P-group.

4.3. Light beam induced current

LBIC scans were performed on five neighbouring cells from a single ingot. The first, third, and fifth wafers were processed according to the standard scheme, the second and the fourth were subjected to an extra anneal at 700 °C for 2 h, with only phosphorus-doped front side and with both phosphorus-doped front and aluminiumdoped back respectively. A scan of 1.0×0.7 cm² was made (see Fig. 6). Dark areas represent regions which give a small local current. The black lines correspond to the metallization pattern. Clearly, these wafers exhibit an identical overall pattern. The scans on cells 1 and 5 (not shown) gave results similar to the scan on wafer 3 (Fig. 6(a)). Striking is the large LBIC signal in the A-group cell (Fig. 6(c)). Not only at the grain boundaries but also in the grains the local effective diffusion length was improved with respect to the unannealed standard cell (see arrows in Fig. 6). In the case when the anneal was performed without an aluminium-doped back side (Fig. 6(b), a smaller increase in diffusion length with respect to the standard cell is observed.



Fig. 6. LBIC scans on three neighbour cells (a) standard cell; (b) P-group cell; and (c) A-group cell annealed at 700 °C for 2 h. The total scan area is 1.0×0.7 cm². The arrows labelled "GB" and "grain" indicate spots at a grain boundary and within a grain respectively, where L_{eff} was enhanced upon annealing. The bar indicates the correlation between the shade of gray and the effective diffusion length in micrometres.

Since the scans in Fig. 6 are performed on cells with almost identical grains, the local effective diffusion length of the standard cell L_{ST} and that of an annealed cell L_{ANN} can be correlated. For all points from the standard cell scan for which $L_{\rm ST}$ lies in a certain interval of width $2\Delta L$ around $L_0 (L_0 - \Delta L < L_{ST} < L_0 + \Delta L)$, the average L_{ANN} of the corresponding points on the annealed cell is calculated. Subsequently, L_{ANN} – L_0 (the increase in local diffusion length due to the thermal treatment) is plotted as a function of L_0 (see Fig. 7). Both for the P cell and for the A cell an increase in local diffusion length is observed for initially small diffusion lengths. The main differences are that this increase is larger in the A cell than in the P cell, and that above



Fig. 7. The increase in local effective diffusion length after a treatment vs the initial effective diffusion length of the standard cell. Shown are averages over the scans of Fig. 6.



Fig. 8. Distribution of cell efficiencies of two groups of 750 cells. Indicated are the FWHM for each group.

 $L_0 = 40 \ \mu m$ the treatment without aluminiumdoped back side (on average) deteriorates the material. For the cell from the A-group, even initial diffusion lengths up to 75 μm are enhanced during the anneal.

4.4. Distribution of cell efficiency

Two large groups of 750 cells were processed: one group as standard cells and the second A-group with an anneal of 700 °C for 1 h. The efficiency distributions (intervals of 0.1%) are shown in Fig. 8. The average efficiency of the standard group and the A-group was 9.90% and 10.24% respectively. The increase in efficiency of 0.34% (absolute) due to the annealing is somewhat smaller than in the two previous groups with equal anneals (see Sections 4.1 and 4.2). The full width at half maximum (FWHM) of the cell efficiency distribution shown in Fig. 8 is 1.05% for the standard group and 0.65% for the A-group. Thus annealing not only improves the average efficiency, but also reduces the width of the efficiency distribution. It is found that the low efficiency tail present in the standard group cell efficiency distribution is virtually absent in the A-group (Fig. 8).

4.5. Concentration of metallic impurities in the aluminium-doped layer

RBS measurements were performed on the monocrystalline CZ samples from the model experiment in the following channelling geometry. The incoming beam of He⁺ ions with an energy of 2 MeV was aligned to the $\langle 100 \rangle$ crystal axis and the backscattering angle was 170° . The results for nickel as the deposited species are shown in Fig. 9. The sample geometry is shown in the inset. The surface channels of oxygen, aluminium, silicon and nickel are indicated. Spectrum I is taken on the control sample after annealing at 700 °C for 1 h. Spectra II and III are measured on aluminium-doped samples which



Fig. 9. RBS spectra of the three sample geometries, shown in the inset, after an anneal at 700 $^{\circ}$ C for 1 h. On sample III, an enhanced signal at the nickel surface channel is observed, whereas virtually no nickel was found on samples I and II.

received an annealing treatment at 700 $^{\circ}$ C for 1 h, without and with nickel deposited on the side opposite the aluminium respectively.

The silicon minimum yield of the aluminiumdoped sample (about 6%) is slightly higher than that of the undoped sample (about 4.5%). This is attributed partly to the presence of aluminium (oxide) at or near the surface, as evidenced by a peak at the aluminium surface channel. It shows that the crystal quality of the aluminium-doped silicon produced by alloying and etching is comparable with that of undoped silicon according to channelling RBS. An increasing yield starting at the nickel surface channel (288) is observed only in spectrum III. The amount of nickel in the surface region can be roughly estimated from the integrated yield between channel 220 and the nickel surface channel 288. For the sample doped with aluminium opposite to the nickel deposited layer (spectrum III) this gives $(15 \pm 1) \times 10^{14}$ atoms cm^{-2} . For the other samples the absence of any clear increase in yield at the nickel surface channel suggests that the amount of nickel in the surface region is very small or negligible. An absolute upper limit for the amount of nickel can be obtained in a way similar to that used for spectrum III. This gives $(3.2 \pm 0.6) \times 10^{14}$ atoms cm⁻² for spectrum II and $(0.8 \pm 0.4) \times 10^{14}$ atoms cm⁻² for spectrum I.

Similar measurements were performed on samples where iron, gold, or copper was deposited instead of nickel (see Table 3). In samples with an aluminium-doped layer opposite to the gold and copper-evaporated layer, increased amounts of these metals were detected after annealing. In all other measurements, the amount of metal impurities at the side opposite to the evaporation side was below the detection limit of RBS. Thus no surface diffusion of the deposited metal or contamination from the ambient occurs

TABLE 3 Concentrations of metallic impurities detected at the side of the wafer opposite to the evaporated metal film after a thermal treatment of 700 °C. Errors are given between parentheses

Geometry Front side Back side			II Metal No aluminium	I No metal Aluminium-doped	III Metal Aluminium-doped	
Metal	$C_{\rm s}$ (cm ⁻³)	$\frac{D}{(\mathrm{cm}^2\mathrm{s}^{-1})}$	Time (h)	$(10^{14} \mathrm{cm}^{-2})$	$(10^{14} \mathrm{cm}^{-2})$	$(10^{14} \mathrm{cm}^{-2})$
Cu	1 × 10 ¹⁶	3×10^{-5}	1	< 5	<10	25 (3)
Nı	3×10^{15}	7×10^{-6}	1	0.8(0.4)	3.2 (0.6)	15.2 (0.6)
Au	4×10^{13}	2.4×10^{-6}	50	0.10(007)	0.17 (0.07)	1.5 (0.2)
Fe	1×10^{11}	4×10^{-7}	50	-	_	< 0.1



^v Fig. 10. SIMS profiles of nickel and aluminium at the back side of the wafer after heating to 700 °C for 1 h Both the aluminium oxide (AlO) and the aluminium signal are a measure of the aluminium concentration.

during the anneal and we conclude that the deposited metal diffuses through the wafer and is gettered in the aluminium-doped layer. Iron has not been detected because the small solubility and diffusivity in silicon (see Table 3) limit the integrated flux through the wafer to a factor 1000 times smaller than the RBS detection limit of iron in silicon.

Secondary ion mass spectroscopy (SIMS) was performed on the aluminium-doped side of the sample from spectrum III in Fig. 9 (see Fig. 10). A clear correlation between the nickel signal and the aluminium signal is observed over more than two decades of concentration.

From simple diffusion theory, using the solid solubility $C_{\rm S}$ and diffusivity D of the particular metallic species in undoped silicon at 700 °C [36] (Table 3), it is calculated that the integrated flux of metal atoms flowing towards the gettering surface opposite to the metal-deposited side is 10 times larger than the observed quantities in the aluminium-doped layer. This suggests that an upper limit of impurity (nickel, gold and copper) concentration in aluminium-doped silicon has been reached. The range from channel 220 to 288 (the nickel surface channel) corresponds to a depth of 0.7 μ m. Dividing the integrated yield between channel 220 and 288 of spectrum III by that depth, the concentration of nickel in the aluminium-doped layer is calculated to be 2×10^{19} cm^{-3} . A similar analysis can be performed for the gold and copper-deposited samples. This yields segregation coefficients (defined as the ratio of the solid solubility $C_{\rm S}$ of the impurity species in intrinsic silicon and the concentration of that species in the gettering region at the gettering

temperature) of less than 10^{-3} for nickel, copper and gold.

5. Discussion

5.1. Emitter efficiency

The emitter quality improves upon annealing, as evidenced by a significant increase in quantum efficiency for wavelengths smaller than 450 nm in both the P-groups and the A-groups annealed at 700 °C. This may be due to several factors.

First, the recombination at the emitter surface may be reduced. In the standard group the emitter surface oxide which is present after phosphorus indiffusion, is not removed until after the aluminium alloying. In a group (not shown here) in which this oxide was removed *prior* to aluminium alloving an increased short wavelength QE compared with that of the standard group was observed. Probably, the emitter surface recombination velocity is improved because of the early removal of this oxide. In the P-groups, the surface oxide was removed prior to the anneal and thus prior to the aluminium alloying, whereas in the A-groups it was removed after the aluminium alloying. The larger QE at small wavelengths (less than 450 nm) of a P-group compared with an A-group with equal anneal time may thus be due to this difference in oxide removal.

Secondly, in the case when the minority carrier diffusion length in the emitter is not limited by band-to-band Auger recombination [37], it may be enhanced by gettering of impurities out of the emitter towards the surface.

Thirdly, a redistribution of the phosphorus doping profile may occur during annealing. From the increasing sheet resistance upon annealing (Fig. 2), it is deduced that either the majority carrier mobility or the active concentration of phosphorus in the emitter decreases with increasing anneal time at 700 °C. Grain boundary diffusion is unlikely to result in a significant reduction of phosphorus. A decrease in the intragrain phosphorus concentration could lead to an improved minority carrier lifetime in the emitter but is ruled out because of the small bulk diffusion length (less than 0.01 μ m) of phosphorus in silicon at 700 °C [38]. Clustering of phosphorus could occur during the anneal at 700 °C, which would result in a decrease in the active phosphorus concentration. If the minority carrier lifetime is limited by band-to-band Auger recombination, such a decrease would result in a lifetime improvement and an enhanced short wavelength QE. However, the effect of clustering on the minority carrier mobility is not clear and this could oppose the enhancement in the QE.

After annealing at 800 °C, R_{sheet} is decreased compared with the 700 °C anneal, which is most likely because of broadening of the emitter profile [8], since the phosphorus solid state diffusion length in silicon at 800 °C after 1 h is equal to 0.05 μ m [39]. The average doping concentration becomes smaller and thereby the majority carrier mobility is enhanced [40]. The emitter minority carrier diffusion length (estimated to be less than 0.2 μ m) is smaller than the emitter thickness. In that case, such broadening results in a decreased small wavelength QE compared with the 700 °C group, as has been observed.

5.2. Base minority carrier diffusion length 5.2.1. Origins of improved diffusion length

From current-voltage measurements, quantum efficiency measurements and LBIC scans, it is found that the bulk effective minority carrier diffusion length increases with increasing anneal time and with increasing anneal temperature up to 700 °C, provided an aluminium-doped back side is present during the anneal. I_{sc} and L_{eft} decrease upon annealing at 800 °C. In the P-groups, annealing at 700 °C results in a smaller increase in L_{eff} with increasing anneal time than in the A-groups.

The mechanisms possibly involved here are an improved back surface recombination velocity, preferential diffusion of aluminium and/or phosphorus along grain and subgrain boundaries, and aluminium-induced and/or phosphorus-induced gettering. These mechanisms will be discussed next.

A reduced back surface recombination velocity S is ruled out as the origin of the increase in L_{eff} because S starts to influence the carrier collection efficiency when the ratio of the minority carrier diffusion length L_{min} to wafer thickness becomes larger than approximately 0.5 [41], whereas in the present case this ratio is in the order of 0.2.

The improved LBIC at the grain boundaries in the A-group cell compared with the standard cell (Fig. 6) may be (partly) caused by preferential aluminium diffusion and/or grain boundary passivation by aluminium. Such preferential diffusion results in a local $p-p^+$ junction by which minority carriers (electrons) are repelled from recombination sites at the boundary [42]. It was found that $L_{\rm eff}$ saturates after annealing for approximately 60 min. This correlates with the aluminium grain boundary diffusion length in silicon which equals the wafer thickness at 700 °C for 60 min [43]. It could be that for prolonged annealing, no significant increase in $L_{\rm eff}$ if observed because the grain boundaries are already decorated with aluminium all through the wafer. Since grain boundaries influence only a small part of the cell area (typically 1%), $L_{\rm eff}$ calculated from the QE measurements will be dominated by intragrain transport parameters and grain boundary recombination reduction can only partly account for the improved $L_{\rm eff}$ upon annealing.

Gettering of impurities is likely to cause the enhanced intragrain diffusion length as observed in the LBIC and QE measurements. The diffusivity of several impurity species at 700 °C is large enough to enable diffusion over a distance of several times the wafer thickness [36, 39]. Solid state diffusion and subsequent passivation of defects by aluminium or phosphorus is ruled out because of the small diffusivity in bulk silicon of aluminium and phosphorus at these temperatures [39]. The FWHM of the cell efficiency distribureduced drastically and LBIC tion was measurements revealed that regions with an initially small L_{eff} are improved most by annealing. If L_{eff} in those regions is limited by some impurity species, removal of that impurity (by gettering) will be most effective in those regions.

Another mechanism which might result in an enhanced minority carrier lifetime is the relief of stress, built into the material during casting or during processing steps such as phosphorus indiffusion. An important factor in such relief will be the cooling rates at the end of the thermal treatments. It was observed that the cooling rate of the extra thermal treatment does not affect the ultimate cell performance for anneal times longer than 30 min [9]. This, however, does not mean that stress relief can be excluded as a factor in the lifetime enhancement.

In the two-diode model of a solar cell, the dark saturation current density and thereby FF and $V_{\rm oc}$ depend on the inverse of the bulk minority carrier diffusion length $L_{\rm min}$ [44] via the first diode prefactor $J_0 \propto 1/L_{\rm min}$ and on space charge recombination and lateral inhomogeneities via the second diode prefactor J_{02} [42]. To a first estimate, neglecting second diode, series resistance, and shunt resistance, the dark saturation

current density is given by $J_0 = I_{sc} \exp(-eV_{oc}/kT)$. Here T is the absolute temperature and k is Boltzmann's constant. Using the data for I_{sc} and $V_{\rm oc}$ from the I(V) measurements to calculate J_0 and using the effective diffusion length $L_{\rm eff}$ (determined by quantum efficiency measurements) which is approximately equal to $L_{\rm min}$, $J_0 \propto 1/L_{\rm eff}$ holds in the A-groups. In the P-groups, this correlation is not obtained, and J_0 even increases with increasing L_{eff} . From this it is concluded that apparently the second diode prefactor increases upon annealing in the P-groups compared with the A-groups. This difference may be explained by an improved lateral homogeneity upon annealing in the A-groups compared with the P-groups. An enhanced homogeneity in the A-groups compared with standard and with P-groups is corroborated by the LBIC measurements, where it was observed that in the A-groups especially the low quality regions are improved most. The analysis becomes more complicated when the shunt and series resistances are incorporated, but the conclusions still hold.

5.2.2. Influence of chemical impurities

Chemical evidence for an enhanced concentration or precipitation of impurities in the aluminium-doped layer was found in the model experiment, which substantiates that an aluminium-doped layer can very well act as an effective sink for impurities at the temperatures involved here. The proof that gettering actually occurs is deduced from the SIMS measurements (Fig. 10). Clearly, the concentration of nickel is larger at the surface than deeper in the sample. Although a correlation between aluminium and nickel concentration was observed, the microscopic mechanism of gettering by aluminium is not yet clear.

The question remains which impurity species may be gettered out of the polycrystalline wafers, either into the phosphorus-doped layer or into the aluminium-doped layer. Since there is an effect of the gettering treatment on the minority carrier diffusion length, it must be a species which limits the recombination lifetime in the material used (*i.e.* Wacker SILSO). Origins of impurities could be the SILSO material, the phosphorus source, the aluminium-containing paste used in screen-printing or the furnace ambients.

The first is unlikely since the measured concentration of most metallic impurities in virgin SILSO has been claimed to be at least an order of magnitude smaller than the permissible solution level [28, 45]. In the furnace, the wafers are in direct contact with a metal belt (consisting of nickel and chromium). The contact between wafer and belt is not a source of contamination during the extra anneal, because no difference in cell efficiency was observed between wafers which were processed with and without direct contact to the belt respectively [10]. Contamination might also occur during phosphorus indiffusion, since a heavy metallic impurity species has been detected (with RBS) at the emitter surface after this processing step. Also, in the aluminium alloy, a small concentration of metallic impurity (iron) was detected prior to etching in aqueous HCl. When a gettering treatment was applied prior to the etching-off of the Al-Si alloy (with its metallic contaminations), cell efficiency and effective minority carrier diffusion length were reduced significantly after annealing at 800 °C [10], possibly because of diffusion of impurities out of the past into the silicon.

5.3. Gettering mechanisms in polycrystalline silicon

An optimum temperature of about 900 °C for most gettering treatments in mono-Si was observed and explained by the diffusion/segregation model [7]. Above that temperature, gettering is limited by the segregation coefficient, defined as the ratio of the solid solubility in the silicon bulk and the maximum impurity concentration in the gettering region. This coefficient increases with increasing temperature. Below the optimum temperature, gettering is limited by the release and diffusion of impurities, which increases with increasing temperature and time. In the present experiments on combined phosphorus-induced and aluminium-induced gettering, a lower optimum temperature of 700 °C was observed. An indication that for phosphorus-induced gettering in poly-Si the optimum gettering temperature is also lower than 900 °C (measured on mono-Si [7]) is the observation that an additional thermal anneal at 700 °C directly after phosphorus indiffusion (which occurs at 875 °C) enhances the final effective minority carrier diffusion length. However, this may also be partly due to relief of stress present in the silicon after the phosphorus indiffusion step.

Several mechanisms might explain the lower optimum gettering temperature in poly-Si.

First, the impurity diffusivity is always larger in

poly-S1 material than it is in mono-Si [38, 46]. Thus the impurity diffusion length exceeds the wafer thickness already for lower temperatures.

Secondly, impurities may be introduced into the material by the processing itself. Higher annealing temperatures may result in larger indiffusion of these extra impurities (see Section 5.2.2), which reduce the minority carrier recombination lifetime.

Thirdly, it was shown that the aluminiumdoped layer can accommodate a large amount of nickel, gold and copper, resulting in a segregation coefficient smaller than 10⁻³ at 700 °C. Segregation coefficients smaller than 10^{-3} have been observed for phosphorus-induced gettering of gold and copper at 1000 °C [24], from which coefficients smaller than 10⁻⁴ at 700 °C are calculated, using the activation energy for the phosphorus-induced gold segregation coefficient [7]. Apparently, the segregation coefficient of the aluminium-doped layer is larger than that of phosphorus-induced gettering. This results in a shift of the aluminium-induced gettering optimum to smaller temperatures, since a segregation coefficient much smaller than unity is needed for effective gettering and this coefficient decreases with decreasing temperature.

From Kang's model, it follows directly that the anneal time will also affect the optimum gettering temperature: the impurity diffusion length is enhanced by increasing the anneal time, but the segregation coefficient remains the same, so longer anneal times would yield smaller optimum temperatures. In our experiments, annealing for 30 min instead of 60 min did not result in another optimum temperature, but our temperature increments of 100 °C restrict the resolution of the optimum temperature to about 50 °C.

It has been suggested that phosphorus- and aluminium-induced gettering are complementary [7, 9, 19]. By comparison of the P-groups with the A-groups, it is clear that the presence of aluminium during the thermal treatment is necessary for optimal improvement of $L_{\rm eff}$. The phosphorus-doped layer getters impurities at 700 °C as suggested by the enhanced $L_{\rm eff}$ upon annealing in the P-groups (where only phosphorus is present during the anneal). This suggests that aluminium getters different impurity species than does phosphorus, which would be a demonstration of the benefit of combined gettering treatments. However, it should be noted here that in the P-groups one side of the wafer is bare during

the anneal, whereas in the A-groups gettering can occur at two wafer surfaces and both surfaces are barriers for ambient impurity indiffusion. Also, part of the improvement in diffusion length upon annealing could be due to stress relief, which may affect groups A and P differently because of the different moments of annealing during the cell processing (Fig. 1).

Another indication of the complementarity is the correlation between the short wavelength QE and the total amount of phosphorus in the emitter [8]. When a gettering step was performed without aluminium, it was observed that only those cells with above average phosphorus emitter concentration were improved. In the case when aluminium was also present during the gettering step, the QE at wavelengths smaller than 600 nm became independent of phosphorus concentration. The interpretation is that a relatively low phosphorus concentration does not effectively getter impurities and only by adding aluminiuminduced gettering are impurities sufficiently removed [8].

Finally, in Kang's experiments the silicon wafers were intentionally doped with impurities at 900 °C prior to the gettering [7], whereas our wafers contain impurities introduced during the casting or subsequent processing steps. Different impurity species exhibit different diffusion behaviour in silicon, so the optimum temperature is not only related to the gettering surface region, but also to the impurity species which is to be gettered. Following this line of thought, it is expected that gettering in materials other than Wacker SILSO also results in an enhanced L_{min} but that the optimum time and temperature may differ from the values presented here.

6. Conclusions

Annealing of polycrystalline silicon wafers, doped at the front side with phosphorus and at the back side with aluminium, was demonstrated to yield an improved effective minority carrier diffusion length. The optimum annealing temperature was approximately 700 °C, which yields an increase of more than 10% in L_{eff} and an absolute efficiency increase of 0.5% resulting in cell efficiencies of 10.4%. The increase in diffusion length is largest at those locations on the cell where L_{eff} is initially small. By diffusion experiments it was shown that impurities such as copper, gold and nickel are effectively gettered at the aluminium-doped layer; the corresponding segregation coefficients are smaller than 10^{-3} at 700 °C.

Based on these observations, it has been argued that gettering of impurities in both the aluminium-doped layer and in the phosphorusdoped layer occurs. The impurities which are gettered may either be present originally in the wafers or be process induced. In the latter case, gettering may be seen as a processing step which reduces the sensitivity of the final cell efficiency to the purity of the process. It should be noted that the aluminium-doping process used in the present study is essentially low cost, unlike previously used metal depositions.

The lower optimum gettering temperature was explained in terms of the larger impurity diffusivity in polycrystalline silicon compared with monocrystalline silicon and the relatively large segregation coefficient of the aluminium-doped layer. For effective gettering, this coefficient should be much smaller than unity, which is the case only at lower temperatures (approximately 10^{-3} at 700 °C). Furthermore, at higher temperatures, contaminants from the ambient may diffuse into the wafers during the thermal treatments, thereby counteracting the effect of gettering. This optimum temperature may be dependent on impurities and may shift to lower temperatures if longer anneal times are applied. The present experiment deals with Wacker SILSO material, but it is expected that aluminium-induced gettering will also be beneficial for other polycrystalline silicon materials.

Acknowledgments

This work is part of the research programme of the Stichting voor Fundamenteel Onderzoek der Materie (FOM, Foundation for Fundamental Research on Matter) and was financially supported by the Nederlandse Organisatie voor Wetenschappelijk Onderzoek (NWO, Netherlands Organization for the Advancement of Science) and by the Stichting voor Technische Wetenschappen (STW, Netherlands Technology Foundation). This project has been carried out partly under contract with the Netherlands Agency for Energy and the Environment (NOVEM) within the framework of the National Research Program Solar Energy-Photovoltaics.

References

- 1 C T. Sah, K. I. Yamakawa and R. Lutwack, *IEEE Trans.* Electron Devices, 29(1982) 903.
- 2 T. Makino and H. Nakamura, Appl. Phys. Lett., 35 (1979) 551.
- 3 C H. Seager and D. S Ginley, J Appl. Phys, 52 (1981) 1050
- 4 K. Nagasawa, Y. Matsushita and S. Kishino, *Appl Phys* Lett, 37(1980)622
- 5 S. M Hu, J. Appl. Phys, 52 (1981) 3974.
- 6 M. L. Polignano, G. F Cerofolini, H. Bender and C Claeys, J. Appl. Phys., 64 (1988) 869.
- 7 J S Kang and D K Schroder, J Appl Phys., 65 (1989) 2974.
- 8 L A. Verhoef, S. Roorda, R. J C. van Zolingen and W. C Sinke, Conf. Record of the 20th IEEE Photovoltaic Specialists Conf., Las Vegas, NV, September 1988, IEEE, New York, 1988, p 1551.
- 9 L. A Verhoef, P.P. Michiels, J. C. Stroom, R. J. C. van Zolingen and W. C. Sinke, in W. Palz, G. T. Wrixon and P. Helm (eds.), Proc. 9th E C Photovoltaic Solar Energy Conf., Freiburg, September 1989, Kluwer, Dordrecht, 1989, p. 733
- 10 S. Roorda, L A Verhoef, W. C. Sinke and R. J. C. van Zolingen, in I. Solomon, B. Equer, and P Helm (eds.), Proc. 8th E C Photovoltaic Solar Energy Conf., Florence, May 1988, Kluwer, Dordrecht, 1988, p. 1446.
- 11 S. Martinuzzi, M. Zehaf, H. Poitevin, G. Mathian and M. Pasquinelli, Conf. Record of the 18th IEEE Photovoltaic Specialist Conf., IEEE, New York, 1985, p. 1127.
- 12 S. Martinuzzi, H. Poitevin, M. Zehaf and C Zurletto, *Rev* Phys. Appl, 22 (1987) 645
- 13 D. Lecrosnier, J Paugam, G Pelous, F. Richou and M Salvi, J Appl. Phys., 52 (1981) 5090
- 14 R D Thompson and K. N. Tu, Appl. Phys. Lett, 41 (1982) 440
- 15 R. Sundaresan, D. E. Burk and J G Fossum, J Appl Phys, 55 (1984) 1162.
- 16 M. C. Chen and V J. Silvestri, J. Electrochem. Soc., 129 (1982) 1294
- 17 P M. Petroff, G. A. Rozgonyi and T T. Sheng, J. Electrochem Soc., 123 (1976) 565
- 18 M. Nakamura, T. Kato and N. Oi, Jpn. J. Appl Phys., 7 (1968) 512
- 19 M. Green, High Efficiency Silicon Solar Cells, Trans Tech Publications, Nedermannsdorf, 1987, p. 214.
- 20 R. Falster, Appl. Phys Lett., 46 (1985) 737.
- 21 A. Ourmazd and W. Schroter, Appl. Phys Lett., 45 (1984) 781
- 22 S L Chou and J. F Gibbons, J. Appl. Phys., 46 (1975) 1197
- 23 R L Meek and T. E Seidel, J Phys Chem. Solids, 36 (1975) 731
- 24 R. L Meek, T E Seidel and A G Cullis, J Electrochem. Soc, 122(1975)786
- 25 R. Bullough and R. C. Newman, in A F. Gibson and R. E. Burgess (eds.), *Progress in Semiconductors*, Vol. 7, Wiley, New York, 1964, p. 99.
- 26 J. Dietl, in C. P. Khattak and K. V. Ravi (eds.), *Materials Processing Theory and Practices*, Vol. 6, North-Holland, Amsterdam, 1987, p. 285.
- 27 T. M. Buck, K. A. Pickar, J. M Poate and C-M. Hsieh, Appl. Phys. Lett., 21 (1972) 485

- 28 D Helmreich, in C. P Khattak and K V Ravi (eds), Materials Processing Theory and Practices, Vol. 5, North-Holland, Amsterdam, 1987, p 97.
- 29 B. Schwartz and H Robbins, J Electrochem Soc, 123 (1976) 1903
- 30 W. K Chu, J W Mayer and M A. Nicolet, *Backscattering Spectrometry*, Academic Press, Orlando, FL, 1978.
- 31 D P Joshi, Solid-State Electron., 29(1986) 19.
- 32 E Fabre, M Mautref and A Mircea, Appl Phys Lett, 27 (1975) 239
- 33 A Agarwal, V K Tewary, S K Agarwal and S. C. Jain, Solid-State Electron, 23 (1980) 1021
- 34 R T. Swimm and K A. Dumas, J Appl Phys., 53 (1982) 7502
- 35 C. Donolato, J. Appl Phys, 54 (1983) 1314.
- 36 E R. Weber, *Properties of Silicon, EMIS Data Reviews* Ser. No 4, INSPEC, New York, 1988, p. 409
- 37 S M Sze, *Physics of Semiconductor Devices*, Wiley, New York, 1981, p. 144.
- 38 H Baumgart, H. J. Leamy, C K. Keller and L E. Trimble, J Phys. (Paris) Colloq C1, 43 (1982) 363

- 39 A S Grove, *Physics and Technology of Semiconductor* Devices, Wiley, New York, 1967, p 38.
- 40 S. M Sze, *Physics of Semiconductor Devices*, Wiley, New York, 1981, p. 29
- 41 H J Hovel, in R. K Willardson and A C. Beer (Eds.), Semiconductors and Semimetals, Vol 11, Academic Press, New York, 1975, p 95
- 42 P. de Pauw, R. Mertens and R van Overstraeten, in C P. Khattak and K V Ravi (eds.), *Materials Processing Theory and Practices*, Vol. 6, North-Holland, Amsterdam, 1987, p 1
- 43 J C M Hwang, P. S Ho, J E Lewis and D R. Campbell, J Appl Phys, 51 (1980) 1576
- 44 S. M Sze, *Physics of Semiconductor Devices*, Wiley, New York, 1981, p 794
- 45 S Pizzini, in C P. Khattak and K. V. Ravi (eds.), Materials Processing Theory and Practices, Vol. 5, North-Holland, Amsterdam, 1987, p 167.
- 46 H J Queisser, K Hubner and W Shockley, *Phys. Rev*, 123(1961)1245